REMARKS

Claims 1-2, 4-7, and 20-30 will be pending upon entry of the present amendment. Claims 1, 4-6, and 29 are being amended. Claim 3 is being cancelled.

Claim 7 was rejected under 35 U.S.C. § 112, second paragraph as being indefinite. Claim 1 is being amended to supply the antecedent basis for "said insulation region" in claim 7. Thus, claim 7 particularly points out and distinctly claims the invention.

Claims 1, 2, and 7 were rejected under 35 U.S.C. § 102 as being anticipated by Ito (JP 09-342878). Claims 3-6, 20-23, and 26-30 were rejected under 35 U.S.C. § 103 as being unpatentable over Ito in view of Sakai (JP 61-232657).

Ito and Sakai do not teach or suggest the invention recited in claim 1, which is being amended to include the elements of cancelled claim 3. Amended claim 1 recites an integrated device with a high-voltage vertical resistor formed by a portion of a semiconductor material body extending between a first and a second surface of the semiconductor material body, and delimited at least partially by an insulation region extending from the first surface towards the second surface of the semiconductor material body. Neither Ito nor Sakai teaches or suggests a vertical resistor delimited by an insulation region extending from the first surface towards the second surface of a semiconductor material body. Instead, Ito shows a resistor R formed in an N-doped region 12b that is laterally surrounded by a P-doped region 13. As for Sakai, Figure 1 of Sakai shows a resistor R as a rectangle that extends lengthwise across the surface of the device and has two small, square contacts also on the surface of the device. As such, the current flow of the resistor R will be horizontal, not vertical, and along the surface of the device between the square contacts.

There is no suggestion or motivation in the art to combine the horizontal resistor of Sakai with the resistor surrounded by the annular P-doped region 13 of Ito to create the claimed invention. The Examiner asserted that it would have been obvious to combine that teaching of Sakai with the resistor of Ito because the Sakai configuration provides an increased electrostatic breakdown capacity. The Examiner is correct that Sakai reports increased breakdown capacity, but that advantage is provided by Sakai's combination of a horizontal

resistor above a vertical PNP transistor surrounded by an insulator 1. Nothing in Ito or Sakai suggests that such an increase in electrostatic breakdown capacity could be provided by anything other than the horizontal resistor/vertical PNP transistor combination. For example, nothing in the art suggests that a combination of Ito's resistor with Sakai's insulation region 11 by itself would provide an increase in electrostatic breakdown capacity or any other benefit. Thus, any teaching borrowed from Sakai would have to include the vertical PNP transistor below the resistor. As discussed in the previous amendment, such a vertical PNP transistor below a resistor causes the current flow in the resistor to be horizontal, rather than vertical.

In view of the above comments, the only possible way to combine Ito and Sakai to arrive at the claimed invention would be to improperly pick and choose from among the elements of Ito and Sakai using hindsight based on the applicant's disclosure. One would have to choose to replace the doped semiconductor region 13 of Ito only with the insulation region 11 of Sakai to obtain Ito's resistor surrounded by Sakai's insulator. Such a hindsight selection would not be based on any teaching in the art and would ignore Sakai's teaching of a vertical PNP transistor below the resistor.

For the foregoing reasons, amended claim 1 is nonobvious in view of the cited prior art.

Claims 4-6 and 29-30 depend on claim 1, and thus, are also nonobvious. In addition, claims 29-30 recite other elements not taught or suggest by Ito and Sakai. In particular, claim 29 recites that the insulating region includes insulating walls made of electrically insulating material and a conductive filler that is laterally surrounded by the insulating walls. An example of such an arrangement can be in Figure 5 of the application in which a conductive filler 34 is surrounded by insulating walls 32. The only insulating region in the cited prior art is the insulating layer 11 of Sakai, which does not include any conductive filler. Thus, claims 29-30 are further distinguished from the cited art.

Claim 30 further recites that the conductive filler is a gate of a transistor that includes source/drain regions in the semiconductor region that is surrounded by the insulating region. The only gate shown in the cited prior art is the gate G shown schematically in Figure 7 of Ito. That gate G is on a surface of a semiconductor 12 and is not a conductive filler of an

insulating region that surrounds a semiconductor region. Thus, claim 30 is further distinguished from the cited art.

Although the language of claims 20-28 is not identical to that of claim 1, the allowability of claims 20-28 will be apparent in view of the above remarks.

Claims 24-25 were rejected under 35 U.S.C. § 103 as being unpatentable over Ito and Sakai in view of U.S. Patent No. 5,229,310 to Sivan.

The cited prior art references do not teach or suggest the invention recited in claims 24-25. In particular, like Sakai, Sivan does not suggest a resistor formed by a doped semiconductor region extending longitudinally into a semiconductor body. Instead, Sivan refers to a vertically oriented thin-film transistor.

Claim 25 further recites that the device includes a transistor having a gate formed by a conductive filler positioned within insulating walls of the insulating region, a first source/drain formed by an upper region of a semiconductor region that is laterally surrounded by the insulating region, and a second source/drain formed by a lower region of the semiconductor region. The cited prior art references do not teach or suggest such a transistor structure. Instead, as discussed above, Ito shows a gate positioned above a surface of a semiconductor substrate. Sakai shows a bipolar transistor having no gate and no source/drain regions. Sivan shows a transistor with a gate 38 formed in a trench 18 and a first electrode 26 formed under the gate 38 in the trench 18. Such a first electrode 26 cannot possibly be either of the first and second source/drain regions recited in claim 25 because the first electrode 26 is not part of a semiconductor region that is laterally surrounded by an insulating region.

The applicant submits that the only way to arrive at the claimed invention from the cited prior art is to improperly pick and choose from those references using the applicant's disclosure as a template. Nothing in either reference suggests a reason to, or how to, convert the bipolar transistor of Sakai to the field effect transistors of Sivan and Ito. Moreover, nothing in either reference suggests taking only the portion of Sivan related to the conductive gate 38 being surrounded by an insulating layer 32 without also positioning the first and second electrodes 26, 28 outside of the insulating layer 32. As discussed above, the first and second source/drain

regions of claim 25 are part of a semiconductor region that is surrounded by the insulating region – not outside of the insulating layer 32 as in Sivan.

For the foregoing reasons, claims 24-25 are nonobvious in view of Sakai and Sivan.

The Commissioner is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

Davide Patti

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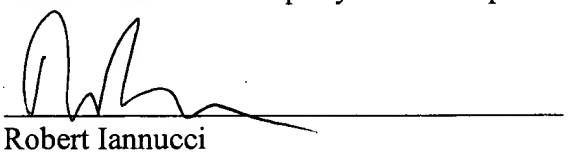

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